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MEASURED EFFECTS OF REPEATER JAMMING
ON DIRECT-SEQUENCE SPREAD SPECTRUM
RECEIVERS THAT USE ENVELOPE DETECTORS

by

Paul Evans

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Thesis Advisor: Glen A. Myers

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signal that allows for correct tracking and therefore will not provide reliable communications.

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Measured Effects of Repeater Jamming On Direct-Sequence Spread Spectrum Receivers that Use Envelope Detectors

by

Paul Evans
Electronics Engineer, Naval Air Test Center
B.S.E.E., The Pennsylvania State University, 1985

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ABSTRACT

The effects of repeater jamming on a direct sequence spread spectrum communications system that uses an envelope detector were experimentally determined. A friendly signal transmitter, jamming signal transmitter, noiseless channel, and receiver were designed, built and tested. The spreading sequences of the friendly and jamming transmitters modulated a carrier to create an on-off keyed (OOK) signal. The OOK signal from the jammer was delayed and added to the friendly signal. The delays ranged from zero to 4 chips, and the J/S ratios ranged from -20 to 20 dB. This signal was then envelope detected and correlated with a replica of the spreading sequence of the transmitters. The results of the correlation show that in instances of high jamming and low jamming, reliable communication should occur. In cases where the jammer power and friendly signal power are nearly equal, the output of the correlator will not produce a signal that allows for correct tracking and therefore will not provide reliable communications.

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NOMENCLATURE

A	Gain of Friendly Signal Amplifier
A_c	Amplitude of Carrier
AGC	Automatic Gain Control
AJ	Anti-Jam
AM	Amplitude Modulation
AVM	Analog Voltage Multiplier
B	Gain of Jammer Amplifier
BPSK	Binary Phase Shift Keying
c(t)	Sinusoidal Carrier
CDMA	Code Division Multiple Access
d(t)	Binary Spreading Sequence
$d_j(t)$	Jammer M-Sequence
$d_s(t)$	Friendly M-Sequence
DC	Direct Current
DLL	Delay Lock Loop
DS	Direct Sequence
e(t)	Unfiltered DLL Error Voltage
ED	Envelope Detector
f_c	Carrier Frequency
FH	Frequency Hopping
$G_s(f)$	PSD of BPSK Signal
HPF	Highpass Filter
J	Jamming Signal Power
J/S	Jamming-to-Signal Ratio
L	Length of M-Sequence

LFSR	Linear Feedback Shift Register
LPF	Lowpass Filter
MSG	M-Sequence Generator
OOK	On-Off Keying
PSD	Power Spectral Density
$r(t)$	Output of Envelope Detector
$R_{xx}(\tau)$	Autocorrelation Function of $x(t)$
$R_{xy}(\tau)$	Cross-Correlation Function Between $x(t)$ and $y(t)$
S	Friendly Signal Power
$s(t)$	Output of Channel Subsystem
SNR	Signal-to-Noise Ratio
T	Bit Interval
T_c	Chip Interval
TH	Time Hopping
$v_e(t)$	Filtered DLL Error Voltage
$v_j(t)$	Jamming Signal
$v_s(t)$	Friendly Signal
VCO	Voltage Controlled Oscillator
$y_1(t)$	Error Voltage With Constructive Interference
$y_2(t)$	Error Voltage With Destructive Interference
$y_3(t)$	Punctual Cross-Correlation With Constructive Interference
$y_4(t)$	Punctual Cross-Correlation With Destructive Interference
δ	Delay of Jammer

I. INTRODUCTION

Spread spectrum systems transmit and receive a signal that has been spread in frequency when compared with conventional digital communications systems. In typical spread spectrum systems, the baseband signal (bit stream) is spread; the result modulates a carrier which is amplified and transmitted. Upon reception, the carrier is demodulated and this output is then despread which results in an estimate of the original bit stream.

The spreading of the spectrum can provide some advantages, such as anti-jam (AJ) protection, code division multiple access (CDMA), or covert communications. If a narrowband jammer is used against a spread spectrum system, the despreading of the friendly signal will spread the power of the jammer over a wider range of frequencies, thus making the jammer less effective. CDMA allows many users to transmit over a single channel by using separate spreading schemes for each user. The receiver only has the despreading code that it needs, so it despreads the message that is intended for it and none of the others. Spread spectrum systems can be covert if the signal is spread sufficiently. If the signal is spread to the point where its power is at or below the level of ambient noise at the receiver, a hostile receiver would not be able to detect the signal. Obviously, these advantages (especially AJ and covertness) are of interest in military communications systems. [Refs. 1 and 2]

The three most popular spectrum spreading techniques are frequency hopping (FH), time hopping (TH), and direct sequence (DS). In frequency hopping, the transmitter transmits a portion of its message on one frequency

then "hops" to another frequency to transmit another portion of the message. The receiver hops synchronously with the transmitter, recovering the entire message. Time hopping spread spectrum involves burst transmission where the initiation and duration of each burst can be varied. In direct sequence spread spectrum, the data modulates another binary sequence that has a higher bit rate than that of the data. This in effect spreads in frequency the power in the signal before transmission. The receiver, using the same spreading sequence, recovers the original message.

In this research, we consider the effects of a repeater jammer on a direct sequence spread spectrum system that transmits via on–off keying. The friendly transmitter, jamming transmitter, channel, and receiver are designed, built, and tested. The output of the receiver correlator is the voltage of interest. The following chapters present the background of direct sequence spread spectrum, the experimental setup, the results of the research and conclusions based on the results.

II. BACKGROUND

The objective of this study is to determine the effect of a repeater jammer on a DS spread spectrum communications system that transmits using AM and receives with an envelope detector. This chapter reviews the principles of DS spread spectrum.

A DS system spreads the frequency spectrum of the transmitted signal by using the binary data stream to modulate another binary sequence that has a bit rate higher than that of the data stream. To avoid confusion, each bit of the spreading sequence is called a "chip." After carrier demodulation, the receiver demodulates the higher rate binary sequence and correlates this with a like locally generated sequence. This in effect "despreads" the signal and provides data recovery.

The typical modulating scheme used with DS systems is binary phase shift keying (BPSK). In this scheme, the data causes the carrier to have 180° phase changes, which is the same as multiplying the carrier by either ±1, or mathematically,

$$s(t) = \pm A \cos(2\pi f_c t). \tag{1}$$

The power spectral density (PSD) of this signal is then given as [Ref. 1, p. 334]

$$G_s(f) = A^2T/4 \{\text{sinc}^2 [\pi(f-f_c)T] + \text{sinc}^2 [\pi(f+f_c)T]\} \tag{2}$$

which is shown in Figure 1 where T is the bit interval. Now if the spreading sequence is included in the signal, the signal can be represented as

$$s_s(t) = \pm A\, d(t) \cos(2\pi f_c t), \tag{3}$$

where d(t) is the binary spreading sequence. The envelope of the power spectral density is then given by

$$G_s(f) = A^2 T_c/4\, [\mathrm{sinc}^2\, [\pi(f-f_c)T_c] + \mathrm{sinc}^2\, [\pi(f+f_c)T_c]], \tag{4}$$

where T_c is the chip interval. Figure 2 shows the power spectral density of this signal where $T_c = T/3$. Figures 1 and 2 demonstrate the concept of spectrum spreading. As seen in the figures, when the spreading sequence was included in the signal, the peaks of the power spectral density decreased by a factor of three, and spread in frequency by a factor of three. As the chip rate of the spreading sequence is increased, the spread of power will also increase. As the spectrum spreads, the signal power density eventually becomes less than the noise level. Therefore, the probability of detecting the occurrence that transmission occurs will decrease. This is important if covert communication is desired.

In the receiver after the carrier is demodulated, the receiver signal may be synchronously multiplied by a replica of the spreading sequence, producing

$$r(t) = \pm A\, d(t)d(t). \tag{5}$$

Since the value of $d(t) = \pm 1$, then $d^2(t) = 1$, and the received signal is despread and ready for data extraction.

The spreading sequence of choice in most spread spectrum systems is a maximal length or m-sequence. These sequences are generated using a linear feedback shift register (LFSR). The length, L, of an m-sequence is 2^n-1, where n is the number of stages in the shift register. The length of the sequence

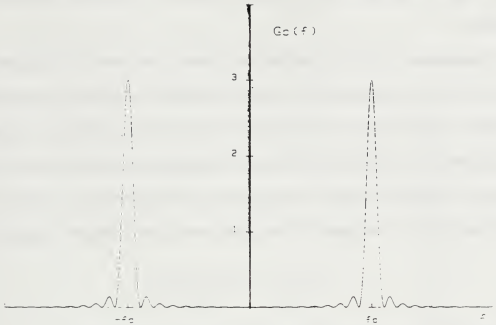


Figure 1. PSD of BPSK Signal

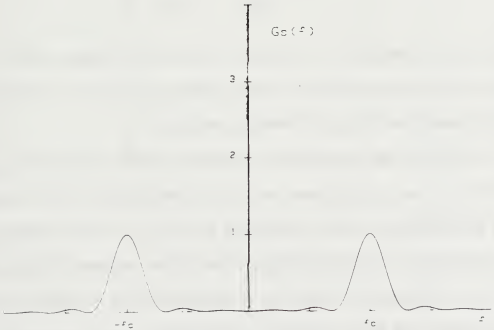


Figure 2. PSD of Spread Signal

used in this experiment is 15 chips. Figure 3 shows one period of this sequence.

M-sequences have properties that make them good candidates for use in spread spectrum systems [Ref. 1, pp. 385-386] lists these properties. Perhaps the most useful of these properties is the autocorrelation function of the m-sequence. The autocorrelation of a function (not limited in time) is the average or expected value of the function multiplied by a delayed value of itself. That is, for a voltage x(t), the autocorrelation function $R_{xx}(\tau)$ is

$$R_{xx}(\tau) = E[x(t)x(t-\tau)]. \tag{6}$$

The normalized autocorrelation of an m-sequence is given by

$$R(\tau) = \begin{cases} 1.0 & \tau = kL \\ -1/L & \tau \neq kL \end{cases} \tag{7}$$

where L is the length of the sequence and k is an integer, and is shown in Figure 4. This autocorrelation function allows the use of a correlator in the receiver to despread the signal for data extraction.

In order for the correlator to operate properly, the locally generated sequence must be synchronous with the incoming signal. This synchronization is accomplished with a delay-lock loop (DLL) whose block diagram is shown in Figure 5. The local LFSR produces three versions of the m-sequence: early, late, and punctual. Typically, the early and late versions are separated by two chips, with the punctual version falling exactly between them. The early and late versions are both correlated with the incoming sequence. The late correlation is subtracted from the early correlation to form the error

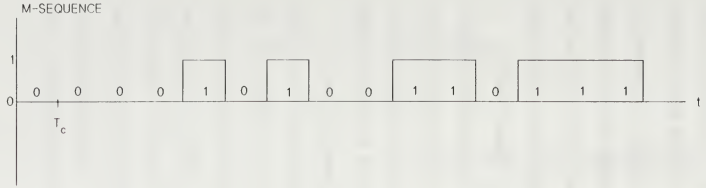


Figure 3. 15 Chip Maximal Length Sequence

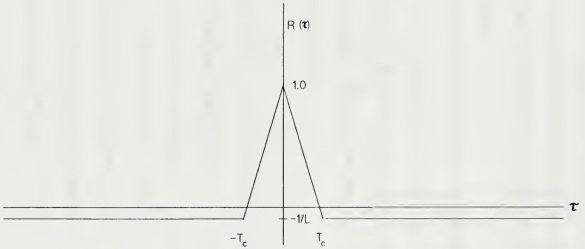


Figure 4. Normalized Auto-Correlation of M-Sequence

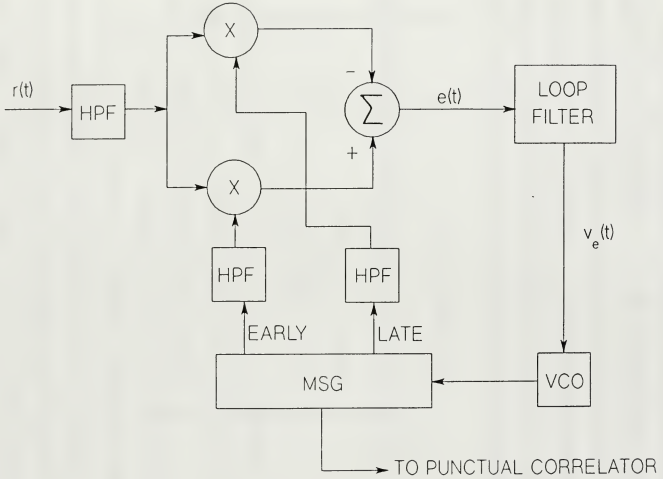


Figure 5. DLL Block Diagram

voltage e(t). This error signal is filtered and then applied to the voltage controlled oscillator (VCO) which is the clock for the m-sequence generator. Because the loop is a closed feedback system, when the VCO frequency matches that of the received sequence, a constant voltage or bias is maintained at the input to the VCO [Ref. 3, p. 44]. At this point, the punctual version of the m-sequence is nearly synchronous with the received signal. So, the output of the punctual correlator is the despread version of the signal, which allows data recovery. [Refs. 3 and 4]

In this research, we consider the use of an envelope detector rather than a coherent demodulator to recover the data modulated m-sequence. Correlation is performed after carrier demodulation. We are interested in the effect a repeater jammer has on the correlator output. Superposition does not apply since the envelope detector is a non-linear device.

A block diagram of the system is shown as Figure 6. The transmitted signal $v_s(t)$ is created by amplitude modulating a unipolar m-sequence, creating an on-off keying (OOK) signal. This transmitted signal is perturbed by a repeater jammer signal $v_j(t)$. The corrupted signal is modeled by adding the amplitude modulated m-sequence to a delayed version of itself to form s(t). This signal is then envelope detected to form r(t). The cross-correlation $R(\tau)$ between the jammed signal and the receiver generated m-sequence is experimentally determined. The effect on system performance of this jamming is also considered analytically.

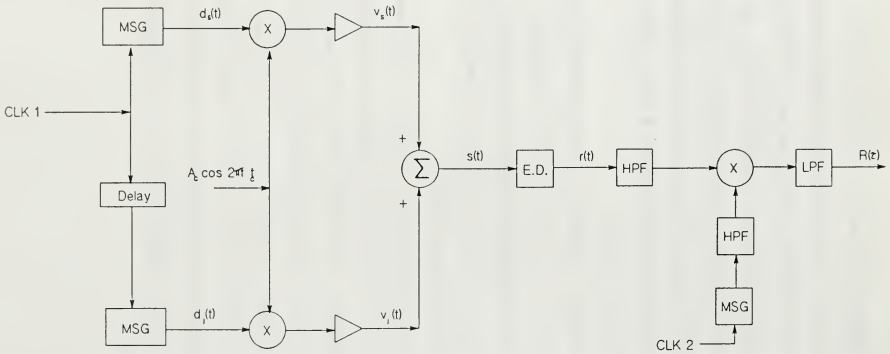


Figure 6. Block Diagram of Experimental System

III. DESCRIPTION AND PERFORMANCE OF THE EXPERIMENTAL SYSTEM

The objective of the experimental system is to model and measure the performance of a typical direct-sequence spread spectrum system operating in the presence of a repeater jammer. Therefore, the experimental system is composed of four subsystems: the friendly signal transmitter, the jamming signal transmitter, the noiseless channel, and the receiver. Each subsystem is discussed separately below. A complete circuit diagram is contained in Appendix A.

A. FRIENDLY SIGNAL TRANSMITTER

The friendly signal transmitter consists of an m-sequence generator and a carrier modulator. Figure 7 is a block diagram of this subsystem. The m-sequence generator (MSG) produces the unipolar binary sequence used to spread any message which has been converted to digital (binary) form. Normally, the data stream "modulates" the m-sequence. However, data is omitted in this experiment since the absence of data has no effect on the results of interest. The MSG consists of a shift register with exclusive NOR (XNOR) logic (74266) implemented in the feedback path. A four stage shift register (74164) generates the sequence, giving a sequence of length $L=2^4-1 = 15$ chips. A [4,1] feedback tap is used. Reference 2 [pp. 87-89] contains a list of feedback taps that produce m-sequences from shift registers of 2 to 89 stages. The upper trace of Figure 8 shows the output of the MSG. A 1.012 kHz main

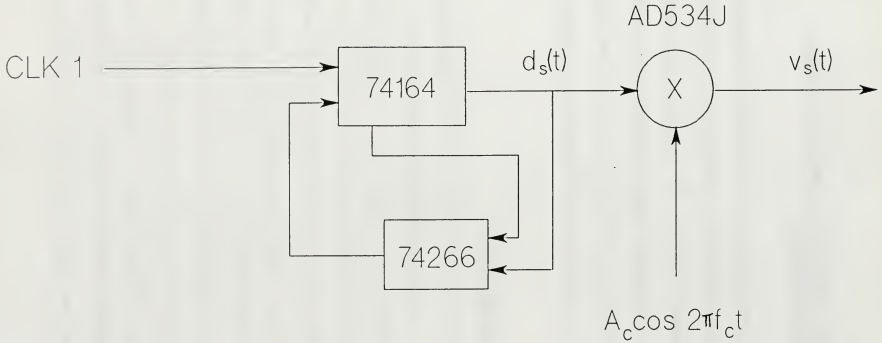


Figure 7. Friendly Signal Transmitter Block Diagram

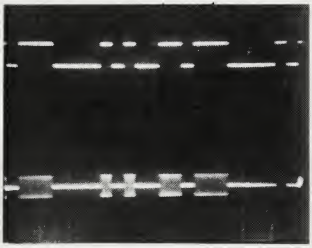


Figure 8. M-Sequence and OOK Version of M-Sequence

(Horizontal Scale: 10 ms/div)
(Vertical Scale: 5 V/div)

clock is applied to a ÷4 circuit to produce the 253 Hz clock that triggers the MSG. The ÷4 circuitry facilitates the required multiples of 1/4 chip delay used in the jamming circuitry.

The output $d_s(t)$ of the MSG is then applied to an AM modulator where it is multiplied by a carrier $c(t)=A_c\cos 2\pi f_c t$ where f_c = 10 kHz. This creates the AM signal

$$v_s(t) = d_s(t)c(t) \tag{8}$$
$$= A_c\cos 2\pi f_c t, \text{ when } d_s(t) = +V = \text{binary 1}$$
$$0, \text{ when } d_s(t) = 0 = \text{binary 0.}$$

This signal is OOK and can be seen on the lower trace of Figure 8.

B. JAMMING SIGNAL TRANSMITTER

The jamming signal $v_j(t)$ used in the experiment models a repeater jammer. This is accomplished by creating a delayed version of the friendly signal. That is,

$$v_j(t) = v_s(t-\delta) \tag{9}$$

where δ is the relative delay the jamming signal incurs due to the reception and subsequent retransmission of the friendly signal. The values of δ used in the experiment are 0, 1/4, 1/2, 3/4, 1, 2, 3, and 4 chips. Since the chip duration T_c is 1/253 = 3.953 ms, the delay of the jammer ranges from 0 to 15.810 ms. Figure 9 is a block diagram of the jamming signal subsystem. The jammer MSG uses the same feedback taps as the friendly signal, and is triggered by the same 253 Hz clock. To produce the 0 chip delay, both MSG's were triggered by the same clock signal. To produce the 1/4, 1/2, and 3/4 chip delays, the ÷2 and ÷4 outputs of the original 1.012 kHz clock are run through

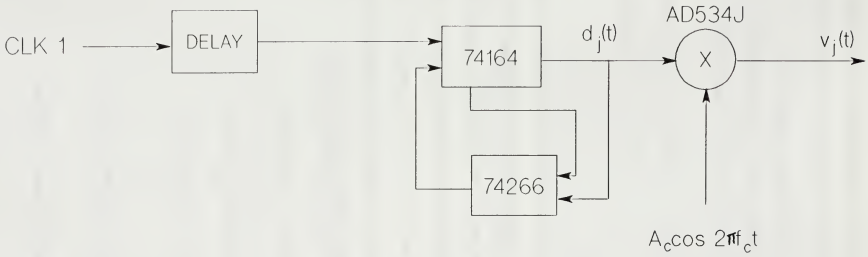


Figure 9. Jamming Signal Transmitter Block Diagram

appropriate logic, whose output then triggers the LFSR of Figure 9. The 1, 2, 3, and 4 chip delays are obtained by using an 8-stage LFSR and using the outputs of the 5th, 6th, 7th, and 8th stages, respectively.

The output $d_j(t)$ of the MSG is then multiplied by the same carrier $c(t) = A_c \cos 2\pi f_c t$ as the friendly signal creating a similar OOK signal

$$v_j(t) = \begin{cases} A_c \cos 2\pi f_c t & \text{, when } d_j(t) = +V = \text{binary 1} \\ 0 & \text{, when } d_j(t) = 0 = \text{binary 0.} \end{cases} \tag{10}$$

C. NOISELESS CHANNEL

The channel subsystem consists of a summing circuit and two amplifiers, as shown in Figure 10. It is a model of the combination of the friendly and jammer signals, with no extra noise introduced. The amplifiers are used to vary the jammer power J to signal power S ratio, J/S. In the experiment, the following five J/S values are used: -20, -10, 0, 10, and 20 dB. Table 1 shows the values of the signal and jammer voltages used to create the specific J/S in the experiment. The J/S are calculated using the equation

$$J/S \text{ (dB)} = 10 \log [J/S]. \tag{11}$$

The output of the channel subsystem s(t) is then

$$s(t) = Av_s(t) + Bv_j(t), \tag{12}$$

where

A = gain of signal amplifier

and

B = gain of jammer amplifier.

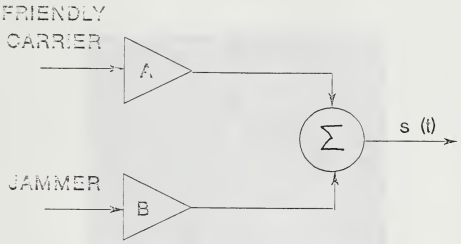


Figure 10. Channel Block Diagram

TABLE I. VALUES OF $v_s(t)$ AND $v_j(t)$ USED TO PROVIDE THE REQUIRED J/S RATIOS

J/S (dB)	$v_s(t)$ (v_{p-p})	$v_j(t)$ (v_{p-p})
-20	24.0	2.4
-10	20.0	6.4
0	6.0	6.0
10	6.4	20.0
20	2.4	24.0

This output is shown in the upper trace of Figure 11, where J/S = 0 dB and the delay is one chip.

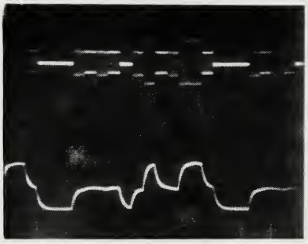


Figure 11. Output of Channel Subsystem With J/S = 0 dB, δ = 1 Chip and Output of Receiver Envelope Detector (Vertical scale: 5v/div) (Horizontal scale: 10ms/div)

D. RECEIVER

The receiver subsystem consists of an envelope detector, an MSG, two highpass filters, and a correlator. Figure 12 shows the block diagram of the receiver subsystem. From Equation (12) and using the expressions for $v_s(t)$ and $v_j(t)$, the input to the receiver is

$$s(t) = AA_c \cos 2\pi f_c t + BA_c \cos 2\pi f_c t \text{ when } d_s(t) = d_j(t) \Rightarrow 1 \quad (13a)$$

$$s(t) = AA_c \cos 2\pi f_c t \text{ when } d_s(t) \Rightarrow 1 \text{ and } d_j(t) \Rightarrow 0 \quad (13b)$$

$$s(t) = BA_c \cos 2\pi f_c t \text{ when } d_j(t) \Rightarrow 1 \text{ and } d_s(t) \Rightarrow 0 \quad (13c)$$

$$s(t) = 0 \text{ when } d_s(t) = d_j(t) \Rightarrow 0 \quad (13d)$$

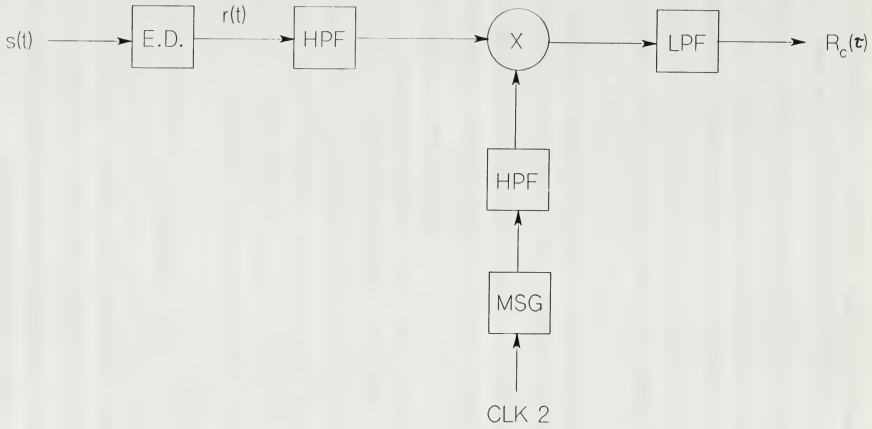


Figure 12. Receiver Block Diagram

From these equations, it is seen that the envelope of r(t) will take on four values, $A_c(A+B)$, AA_c, BA_c, and 0. Therefore the output of the envelope detector will be a four-level voltage. In the case of J/S = 0 dB, the output will be a three-level voltage since A = B. This voltage is shown in the lower trace of Figure 11 for J/S = 0 dB. The output of the envelope detector is then highpass filtered in order to remove the DC component of the signal. Removal of the DC component is necessary to produce the correct (bipolar) input to the correlator.

The second input to the correlator is obtained from another MSG. This MSG has the same feedback taps as the friendly signal and jammer signal; therefore, it produces the same sequence. This sequence is clocked at a rate of 242 Hz, which allows the two correlator inputs to slide by each other when producing the cross-correlation function. Again, the output of this MSG is highpass filtered to remove the DC component before correlation.

The correlator portion of the receiver consists of an analog voltage multiplier (AVM) and a lowpass filter. The cutoff frequency of the lowpass filter must be high enough to pass the difference in frequency between the signal chip rate and the chip rate of the MSG in the correlator. The cross-correlation function is the average of the multiplication of one signal and the delayed version of another signal,

$$R_{xy}(\tau) = E[x(t)y(t-\tau)]. \tag{14}$$

This cross-correlation is a function of the time delay τ. The output of the correlator, the cross-correlation function of the jammer + signal and the friendly signal, is the voltage of interest in this experiment. The output of the correlator is displayed on an oscilloscope and photographed.

IV. RESULTS AND DISCUSSION

Photographs of the voltage representing the cross-correlations of interest are shown in Figures 13 through 23. For each tested value of J/S, there are nine figures included. The first figure in each J/S group is the correlator output with no jamming included and with the signal voltage set to the value used in the remaining experiments. These figures serve as a reference when observing the change in shape or amplitude of the correlation peak. The remaining eight figures in each group show the output of the correlator with the jammer delayed by 0, 1/4, 1/2, 3/4, 1, 2, 3, and 4 chips. The cross-correlation function is periodic, but only one period is shown to improve the time resolution of the oscilloscope display. All correlator outputs are photographed with the following fixed parameters:

Friendly Signal Chip Rate	= 253 Hz
Jamming Signal Chip Rate	= 242 Hz
Vertical Scale	= 0.1 V/div
Horizontal Scale	= 0.2 sec/div
Centerline Value	= 0.1 V.

A. JAMMING-TO-SIGNAL RATIO OF -20 dB, FIGURES 13 AND 14

The peak value of the correlation voltage (no jamming) is approximately 0.4 V, and the width of the peak at the zero volt level is approximately 1.6 divisions, or 0.32 s. When the jamming is added with no delay, the cross-correlation is virtually the same as the auto-correlation, as is expected since the

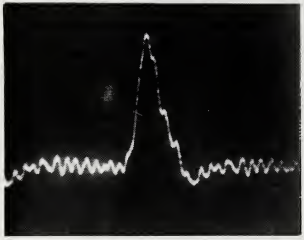
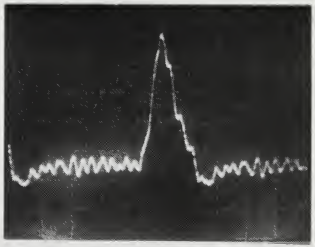
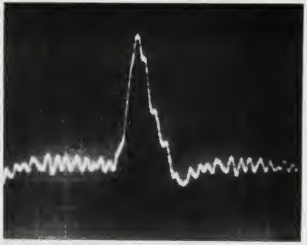


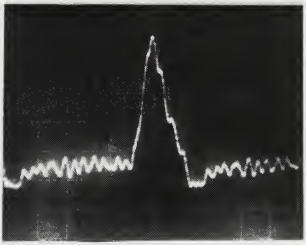
Figure 13. Reference Correlator Output With No Jamming for J/S= -20 dB Case



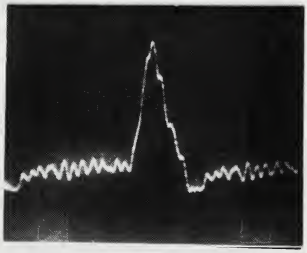
(a) δ = 0 chips



(b) $\delta = \frac{1}{4}$ chip

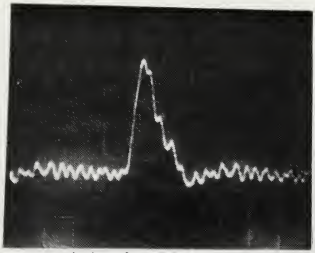


(c) $\delta = \frac{1}{2}$ chip

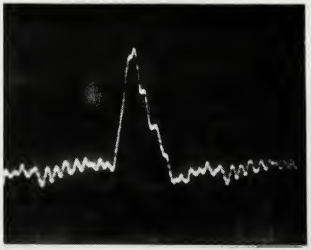


(d) δ = 3/4 chip

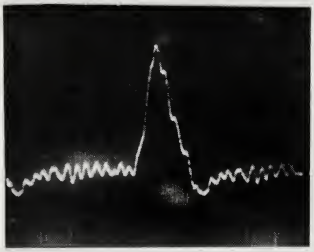
Figure 14. Correlator Output With J/S= -20 dB and Varying Delay



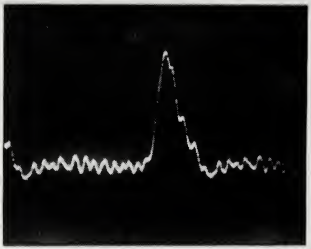
(e) δ = 1 chip



(f) δ = 2 chips



(g) δ = 3 chips



(h) δ = 4 chips

Figure 14. (cont.)

jammer is actually adding in phase with the signal. As the jamming signal is delayed, slight changes occur in the correlator output. The peak value of the function decreases slightly, to a minimum of approximately 0.35 V. The width of the peak at zero volts increases to approximately 1.8 divisions, or 0.36 s at a jammer delay of 1 chip. The width at delays greater than 1 chip returns to 0.32 s. This suggests that another peak due to the jamming signal is occurring, but it is smaller than the resolution of the display. In this scenario, it would seem that a delay-lock loop (DLL) would have little difficulty in acquiring or tracking the incoming signal. Thus, this level of jamming is ineffective.

B. JAMMING-TO-SIGNAL RATIO OF -10 dB, FIGURES 15 AND 16

The peak value of the correlation voltage is approximately 0.4 V, and the width of the peak at zero volts is approximately 0.36 s. Again, the addition of jamming at no delay does not change the output. As the delay in the jammer increases, the peak value decreases and the width of the pulse increases slightly. The peak value decreases to a minimum of approximately 0.26 V at a delay of four chips. The width increases to approximately 0.36 s at a delay of one chip. At this J/S the peak from the jammer begins to appear. The peak of the function at this J/S is lowered considerably more than at a J/S of -20 dB. Although the effect of the jammer is more apparent, a DLL should still be able to acquire and track reliably.

C. JAMMING-TO-SIGNAL RATIO OF 10 dB, FIGURES 17 AND 18

The peak value of the correlation voltage is approximately 0.18 V and the width of the peak at zero volts is approximately 0.36 s. When the jamming is added with no delay, the peak value increases to approximately 0.4 V,

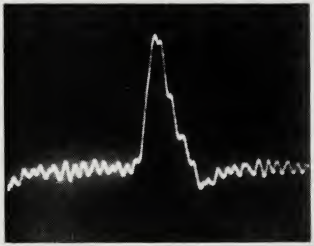
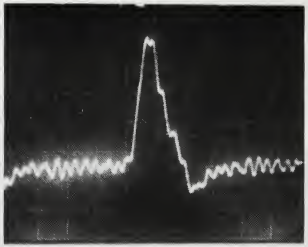
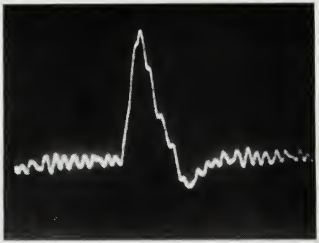


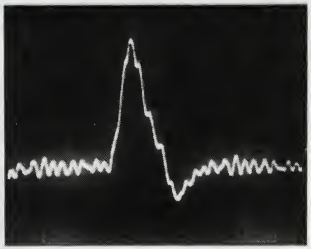
Figure 15. Reference Correlator Output With No Jamming for J/S= -10 dB Case



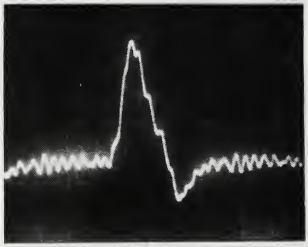
(a) δ = 0 chips



(b) $\delta = \frac{1}{4}$ chip

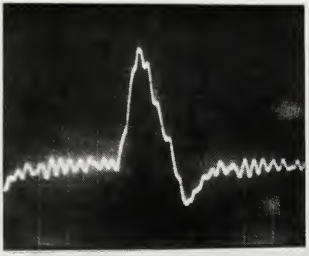


(c) $\delta = \frac{1}{2}$ chip

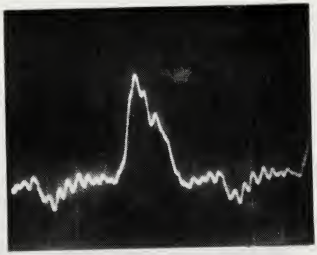


(d) δ = 3/4 chips

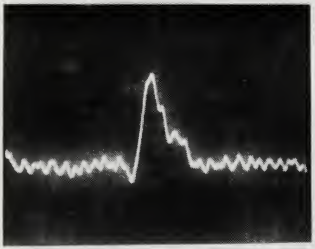
Figure 16. Correlator Output With J/S= -10 dB and Varying Delay



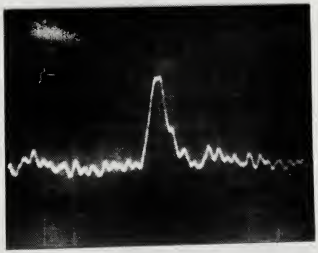
(e) δ = 1 chip



(f) δ = 2 chips



(g) δ = 3 chips



(h) δ = 4 chips

Figure 16. (cont.)

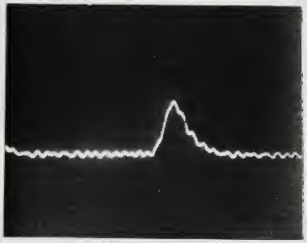
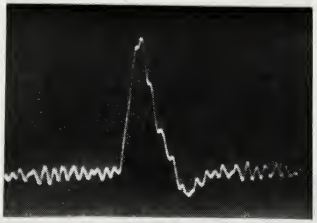
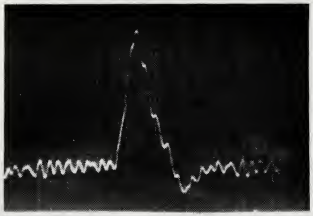


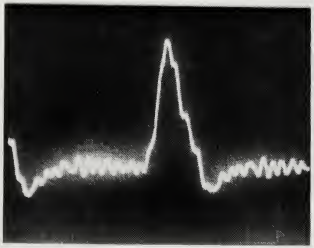
Figure 17. Reference Correlator Output With No Jamming for J/S= 10 dB Case



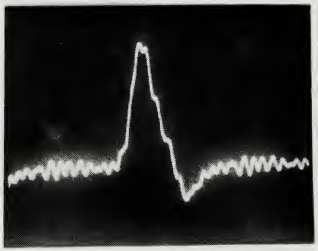
(a) δ = 0 chips



(b) $\delta = \frac{1}{4}$ chip

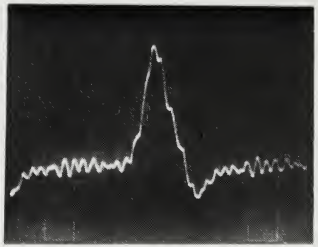


(c) $\delta = \frac{1}{2}$ chip

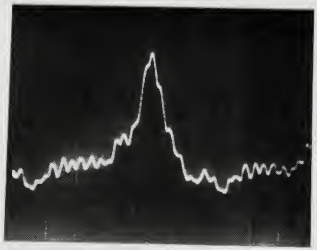


(d) δ = 3/4 chip

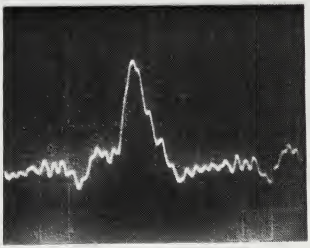
Figure 18. Correlator Output With J/S= 10 dB and Varying Delay



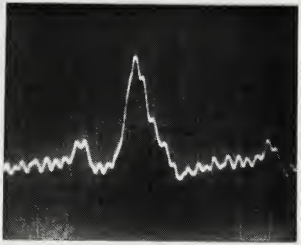
(e) δ = 1 chip



(f) δ = 2 chips



(g) δ = 3 chips



(h) δ = 4 chips

Figure 18. (cont.)

since the jamming voltage is larger than the signal voltage. Therefore, the peak due to the jammer should be larger than that of the signal. As the jammer is delayed, the width of the peak due to the jammer increases until the delay reaches 1 chip. For larger delays, the peak due to the friendly signal becomes visible. Since the amplitude of the jammer peak is large compared with that of the signal, the DLL can be expected to eventually lock on to the jammer signal. Even though the DLL synchronizes with the jamming signal, data recovery will not be affected provided the jamming signal is a time replica of the friendly signal.

D. JAMMING-TO-SIGNAL RATIO OF 20 dB, FIGURES 19 AND 20

The peak of the correlation voltage is approximately 0.08 V, and the width of the peak is approximately 0.36 s. When the jammer is applied, the peak increases to a value of approximately 0.42 V. As the jamming signal gets delayed, it is seen that the peak is due to the jamming signal. As the delay increases, the peak due to the friendly signal can be seen. Again, since the peak due to the jamming signal is so large compared to that of the friendly signal, the DLL will lock on to the jamming signal. As in the 10 dB J/S case, synchronization with the jammer will not affect data recovery if the jammer is a time replica of the friendly signal.

E. JAMMING-TO-SIGNAL RATIO OF 0 dB, FIGURES 21 THROUGH 23

The peak value of the correlation voltage is approximately 0.15 V and the width of the peak at zero volts is approximately 0.32 s. When the jamming is added at no delay, the peak value rises to approximately 0.3 V. This

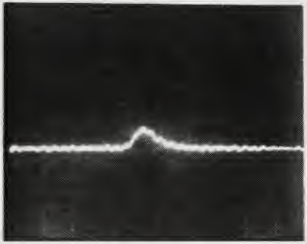
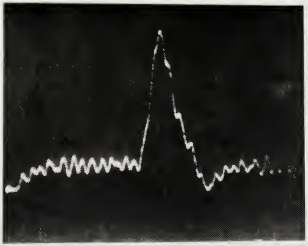
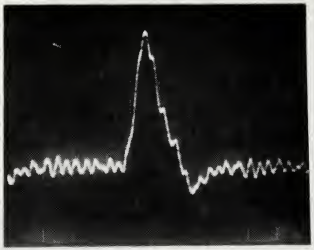


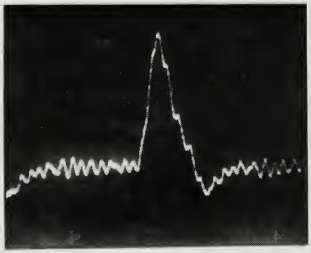
Figure 19. Reference Correlator Output With No Jamming for J/S= 20 dB Case



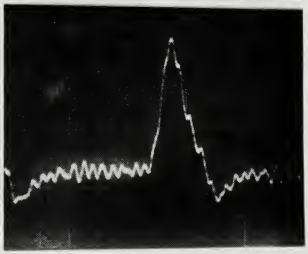
(a) δ = 0 chips



(b) $\delta = \frac{1}{4}$ chip

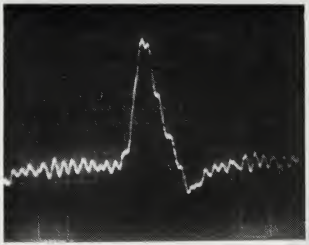


(c) $\delta = \frac{1}{2}$ chip

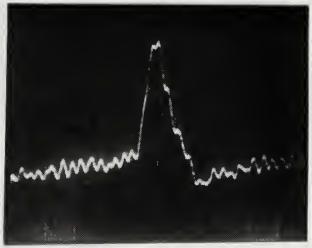


(d) δ = 3/4 chip

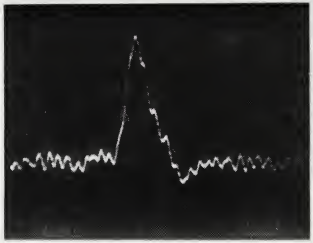
Figure 20. Correlator Output With J/S= 20 dB and Varying Delay



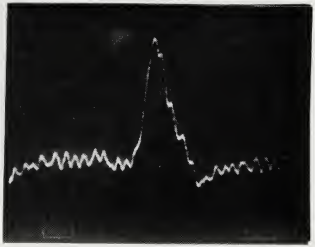
(e) δ = 1 chip



(f) δ = 2 chips



(g) δ = 3 chips



(h) δ = 4 chips

Figure 20. (cont.)

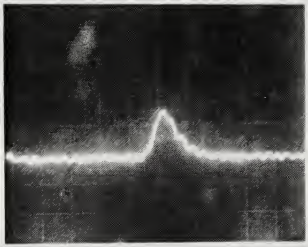
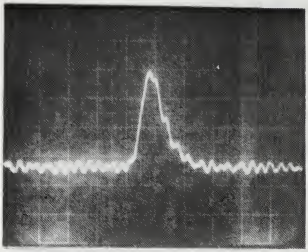
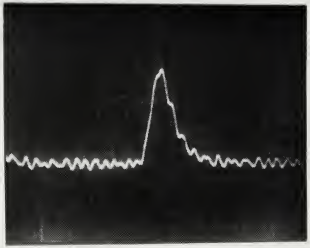


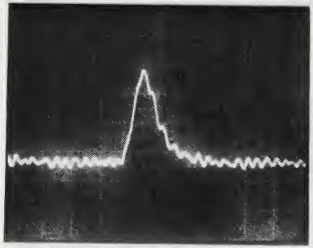
Figure 21. Reference Correlator Output With No Jamming for J/S= 0 dB Case



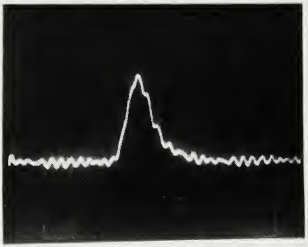
(a) δ = 0 chips



(b) $\delta = \frac{1}{4}$ chip

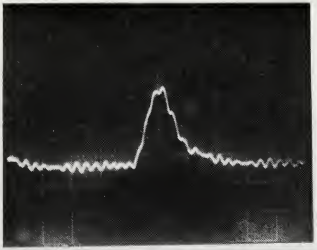


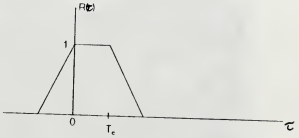
(c) $\delta = \frac{1}{2}$ chip



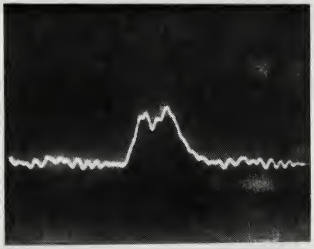
(d) δ = 3/4 chip

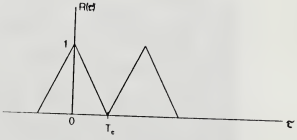
Figure 22. Correlator Output With J/S= 0 dB and Varying Delay





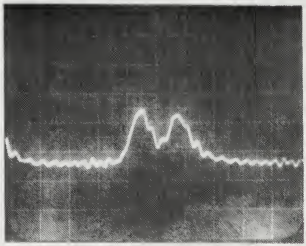
(a) δ = 1 chip

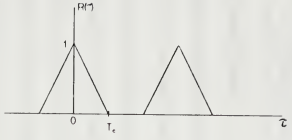




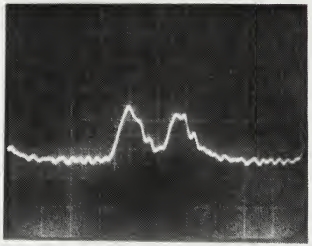
(b) δ = 2 chips

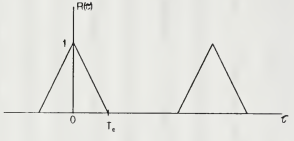
Figure 23. Experimental and Theoretical Correlator Output With J/S= 0 dB and Varying Delay





(c) δ = 3 chips





(d) δ = 4 chips

Figure 23. (cont.)

is expected since the addition of the jammer is double the voltage due to the signal. Again, as the jammer delay increases, the main peak decreases and the peak begins to spread slightly. At a jammer delay of two chips, two separate peaks become visible, and, as may be expected, the time interval between the two peaks increases with increasing jammer delay. The theoretical cross-correlation function is included with the figures for delays of 1, 2, 3, and 4 chips. As can be seen, the experimental cross-correlation voltages closely match the predicted values. The cross-correlation at delays of less than one chip should not cause any problems with data recovery. Jammer delays of one chip and greater, though, may impair data recovery. If the theoretical cross-correlation function are used to create the error voltage in a DLL, then these error voltages will not always provide the correct signal to the VCO. The error voltage generated at a jammer delay of one chip will incorrectly clock the VCO since the zero crossing of this voltage is greater than one chip. The error voltage generated at two chips delay will not allow the DLL to track properly due to the zero slope portion. The error voltages generated from the three and four chip delays may or may not produce the required frequency on the VCO depending on the initial conditions. Therefore the recovered data may be incorrect. Since most repeater jamming would have delays greater than one chip, use of the repeater jammer at 0 dB J/S would seem to be the most effective in the communications system modeled.

V. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

In this research, a DS spread spectrum system that uses OOK was designed, built and tested. The transmitted signal was perturbed by a repeater jammer before it was applied to a receiver, and the cross-correlation function between the friendly signal and the friendly + jamming signal was measured. For J/S values of -20 and -10 dB at any delay, the receiver and DLL should work properly. For J/S values of 10 and 20 dB at any delay, the receiver will synchronize with the jammer signal, but since this is an exact replica of the friendly signal, the receiver and DLL should work properly. At J/S of 0 dB, reliable operation of the receiver will depend on the amount of jammer delay. At delays less than one chip, the receiver and DLL should work properly. At delays of one chip and above, operation of the DLL will be unreliable and recovered data may not be valid.

Fading caused by interference due to the phase relationship between the signal and jammer was not considered in the experimentation. An analysis of this fading is presented in Appendix B. The decrease in signal-to-noise ratio caused by the fading will result in an increased bit error ratio at the receiver.

B. RECOMMENDATIONS

It is recommended that a DS spread spectrum system be used in radios that have envelope detectors only in scenarios where high or low power repeater jammers are being utilized.

A DLL should be designed and constructed and should be tested with the system designed in this research to provide experimental data to be compared with the theoretical error voltages considered here.

APPENDIX A

DETAILED CIRCUIT DESIGN

This appendix presents the circuit diagrams for the friendly signal transmitter, jamming signal transmitter, channel, and receiver used in this experiment.

A. FRIENDLY SIGNAL TRANSMITTER

The friendly signal transmitter consists of an m-sequence generator and an analog voltage multiplier (AVM). The circuit diagram is shown in Figure A-1. The Q_A and Q_D outputs of a 74164 shift register are applied to the inputs of a 74266 XNOR gate and fed back into the A and B inputs of the 74164 to produce the m-sequence. The m-sequence is obtained at the Q_D output of the 74164. This is then applied to the X_1 input of the AD534J AVM. The other input of the AVM is the modulated carrier, cos $2\pi f_c t$ where f_c = 10 kHz. The output of the AVM is the friendly OOK signal. The clock that controls the 74164 is obtained from the circuit shown in Figure A-2. A 1012 Hz square wave is applied to a ÷4 circuit to produce a 253 Hz square wave to clock the 74164. The ÷4 circuit consists of a 74109 dual J-$\overline{K}$ flip flop. The J and $\overline{K}$ inputs of each flip flop are configured to produce a toggling action, and the 1012 Hz clock is applied to the CLK1 input of the 74109. The Q1 output of the 74109 is then applied to the CLK2 input which produces the required 253 Hz clock at the Q2 output.

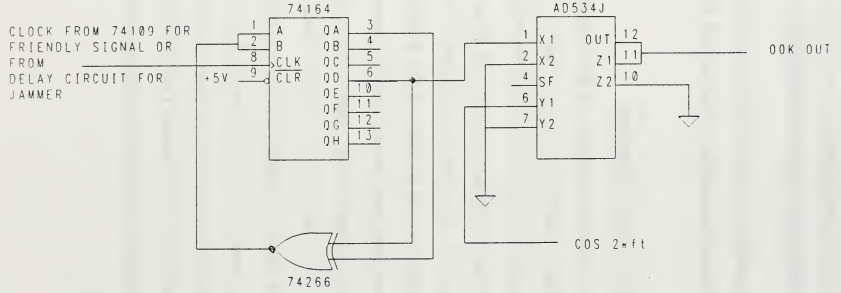


Figure A-1. Friendly and Jamming Signal Transmitter Circuit Diagram

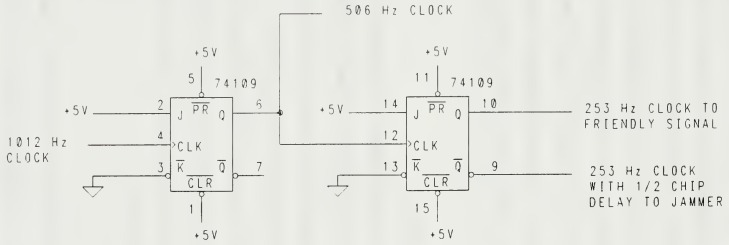


Figure A-2. Clocking Circuit for Friendly and Jamming Signals

B. JAMMING SIGNAL TRANSMITTER

The jamming signal transmitter is constructed the same way as the friendly signal transmitter shown in Figure A-1. The difference between the signals is that the jamming signal must be delayed. To obtain this delay, the clocking circuit of Figure A-2 is modified. For 0 chip delay, the jammer is clocked with the same clock as the friendly transmitter. To provide a 1/4 chip delay, the Q2 and Q2 outputs of the 74109 are applied to a 7486 XOR gate as shown in Figure A-3. The 1/2 chip delay is obtained by using the Q2 output of the 74109 as the clock. The 1, 2, 3, and 4 chip delays are created by using the Q_E, Q_F, Q_G, and Q_H outputs, respectively, of the jamming signal 74164 as the input to the AVM.

C. NOISELESS CHANNEL

The channel modeled for this experiment consists of two amplifiers and a summing circuit. The circuit diagram is shown in Figure A-4. The friendly and jamming signals are applied separately to LM741 operational amplifiers (OP AMPS) configured as non-inverting amplifiers. The 101 kΩ variable resistors are used to adjust the gain of the amplifiers to produce the required J/S ratios. The outputs of these amplifiers are then applied to another LM741 OP AMP configured as a summing amplifier, which produces the addition of the friendly and jamming signals.

D. RECEIVER

The receiver constructed for this experiment consisted of an envelope detector and a correlator. The envelope detector consisted of a 1N645 diode, a 10 kΩ resistor, and a 0.01 μF capacitor as shown in Figure A-5. The output of

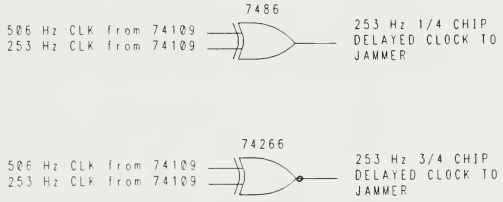

7486
506 Hz CLK from 74109
253 Hz CLK from 74109
253 Hz 1/4 CHIP DELAYED CLOCK TO JAMMER
74266
506 Hz CLK from 74109
253 Hz CLK from 74109
253 Hz 3/4 CHIP DELAYED CLOCK TO JAMMER

Figure A-3. 1/4 and 3/4 Chip Delay Circuits

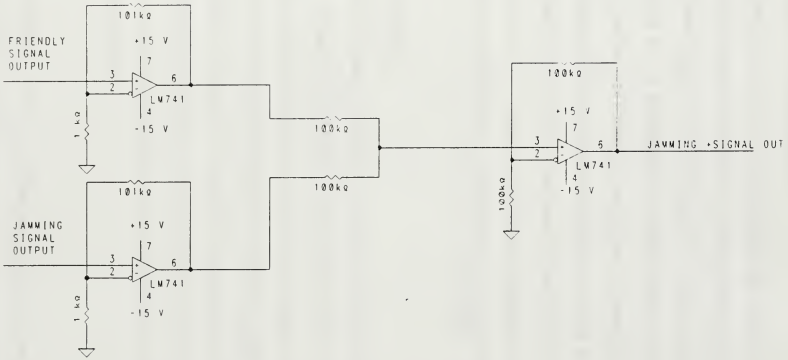


Figure A-4. Channel Circuit Diagram

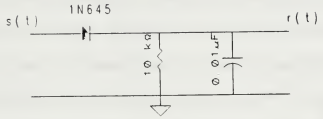


Figure A-5. Envelope Detector Circuit Diagram

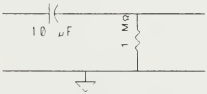


Figure A-6. HIghpass Filter Circuit Diagram

the envelope detector is then applied to a highpass filter to remove the DC portion of the signal in preparation for correlation. The filter has a cutoff frequency of 0.02 Hz and is shown in Figure A-6. The bipolar output of the envelope detector is then applied to the correlator, as shown in Figure A-7. The correlator consists of an AVM and a four stage lowpass filter. The second input to the AVM is a bipolar m-sequence. The sequence in the receiver is the same as the m-sequence generated in the transmitters, but with a clock frequency of 242 Hz. This m-sequence is made bipolar by using a highpass filter as shown in Figure A-6. The output of the AVM is then applied to the lowpass filter whose cutoff frequency is 9.95 Hz. The output of this filter is the cross-correlation function that is analyzed in the report.

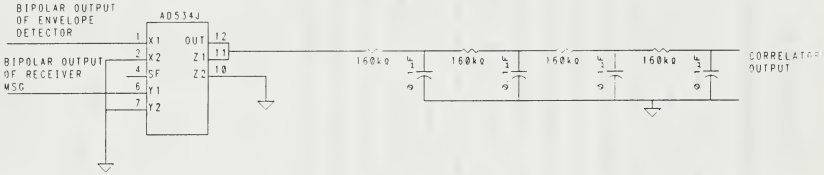


Figure A-7. Correlator Circuit Diagram

APPENDIX B

FADING ANALYSIS

This appendix provides a short analysis of the operation of a direct sequence spread spectrum receiver when fading caused by the jammer (or multipath) due to constructive or destructive interference occurs. When the jamming signal is exactly in phase with the friendly signal, these signals will constructively interfere and produce a correlator output that is larger by k volts than the correlator output with no jamming. Conversely, when the two signals destructively interfere, the correlator output is less than the original output by k volts. (Here, $k < 1$.) Figure B-1 illustrates this by showing the error voltage produced by the DLL as well as the punctual correlator output. The error voltage produced with constructive interference is denoted $y_1(t)$, the error voltage produced with destructive interference is $y_2(t)$. The punctual correlator output produced with constructive interference is $y_3(t)$, and the punctual correlator output produced with destructive interference is $y_4(t)$. The equations of these lines in the area of interest ($-T_c < t < 0$) are as follows:

$$y_1(t) = -\left(\frac{1+k}{T_c}\right) t \tag{B.1}$$

$$y_2(t) = -\left(\frac{1-k}{T_c}\right) t \tag{B.2}$$

$$y_3(t) = \frac{1+k}{T_c}\, t + (1+k) \tag{B.3}$$

$$y_4(t) = \frac{1-k}{T_c}\, t + (1-k) \tag{B.4}$$

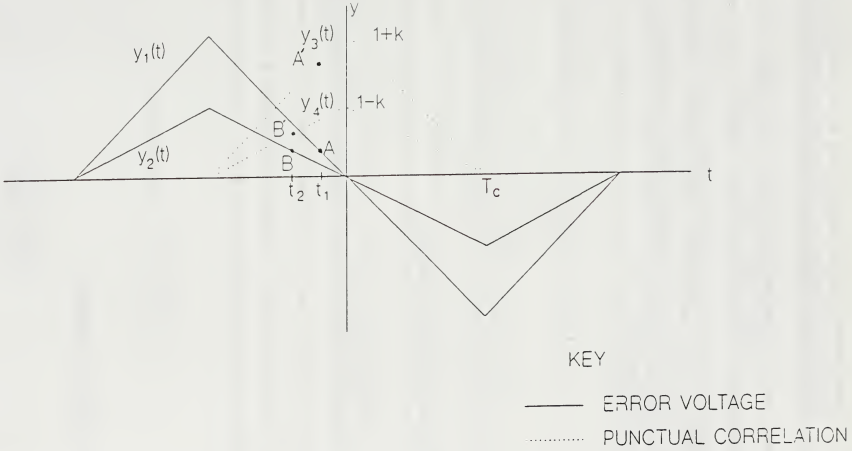


Figure B-1. DLL Error Voltage and Punctual Correlator Output with Constructive and Destructive Interference

We wish to determine the loss in signal power at the receiver due to fading. Assume the voltage A is required to obtain lock of the DLL when constructive interference occurs. The output of the punctual correlator is then the voltage A. With destructive interference, the same voltage B = A is needed for the DLL. Now the output of the punctual correlator is the voltage B. This dB loss of signal power is 20 times the logarithm of the ratio of the voltages at points B' and A' on the figure. So,

$$y_1(-aT_c = t_1) = a(1+k) > 0 = A = \text{operating point} \qquad \text{(B.5)}$$

$$y_2(t) = a(1+k) = -\left(\frac{1-k}{T_c}\right) t \text{ when } t = -aT_c\left(\frac{1+k}{1-k}\right) < 0 \qquad \text{(B.6)}$$

Now, B' in the value of $y_4(t)$ when $t=t_2$

$$\therefore B' = \left(\frac{1-k}{T_c}\right)\left(\frac{1+k}{1-k}\right)\left(-aT_c\right) + 1-k = -a(1+k) + 1-k \text{ where } \begin{matrix}0<a<0.5\\0<k<1\end{matrix} \qquad \text{(B.7)}$$

Note that it is necessary that B' which is less than 1-k be greater than B. That restricts a to be less than 0.5. Now, A' is the value of $y_3(t)$ with $t = t_1 = -aT_c$

$$\therefore A' = \left(\frac{1+k}{T_c}\right)\left(-aT_c\right) + (1+k) = (1+k)(1-a) > 0 \qquad \text{(B.8)}$$

Therefore a dB loss in signal of

$$20 \log \left(\frac{1-k}{1+k}\right)$$

due to fading produces a signal-to-noise ratio (SNR) loss in dB of

$$20 \log \left(\frac{B'}{A'} \right) = 20 \log \left[\frac{-a(1+k) + 1-k}{(1-a)(1+k)} \right]$$

For example, when a = 0.1 and k = 0.1 = -20 dB, then the loss in SNR is 1.94 dB. If a = 0.1 and k = 0.7 = -3 dB, the SNR loss is 22 dB. (Note that a < 0.5 for all k; also, it is necessary that A < 1-k. This means a is such that $y_1(-aT_c)$ < 1-k or a(1+k) < 1-k or

$$a < \frac{1-k}{1+k}$$

Otherwise, the argument of the logarithm < 0, and the DLL will not lock.)

This loss in SNR will correspond to an increased bit error ratio and therefore degrade performance in an operating system. The use of an automatic gain control (AGC) circuit can be used to overcome fading when the signal power is greater than the noise power. If the signal power is less than the noise power (covert communication), the use of AGC is probably not practical.

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3. Hanratty, Joseph Michael, "Measured Noise Performance of a Delay Lock Tracking Loop When Noise Power Exceeds Signal Power," Master's Thesis, Naval Postgraduate School, Monterey, California, 1982.

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